MARKED UP COPY OF AMENDED CLAIMS

1. (Thrice Amended) A semiconductor device comprising a first semiconductor chip and a second semiconductor chip superposed on and bonded to a surface of the first semiconductor chip,

wherein, in a chip bonding region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip, chip connection portions are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips,

wherein, on the second semiconductor chip, chip connection portions are arranged so as to fit the chip connection portions arranged on the first semiconductor chip at least for one of the plurality of predetermined types of semiconductor chips, and

wherein the chip connection portions arranged on the first semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along [one] a first side of [the] said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along [one] said first side of [the] said at least one pair of opposite sides to the chip connection portions arranged along [the other] a second side of [the] said at least one pair of opposite sides, and at least part of the chip connection portions arranged on the first semiconductor chip are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

3. (Thrice Amended) A semiconductor chip having, on a surface thereof, a chip bonding region that fits one of a plurality of predetermined types of semiconductor chips,

wherein, in the chip bonding region, chip connection portions are arranged in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and

wherein the chip connection portions arranged on the semiconductor chip are arranged along at least one pair of opposite sides of the chip bonding region, a distance between the chip connection portions arranged along [one] a first side of [the] said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along [one] said first side of [the] said at least one pair of opposite sides to the chip connection portions arranged along [the other] a second side of [the] said at least one pair of opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.

10. (Thrice Amended) A semiconductor chip having, on a surface thereof, a chip connection region that fits any of a plurality of predetermined types of semiconductor chips,

wherein, in the chip connection region, chip connection portions are formed in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connection portions are arranged along an edge of the chip connection region, and

wherein the chip connection portions are arranged along at least one pair of opposite sides of the chip connection region, a distance between the chip connection portions arranged along [one] a first side of [the] said at least one pair of opposite sides is shorter than a distance from the chip connection portions arranged along [one] said first side of [the] said at least one pair of opposite sides to the chip connection portions arranged along [the other] a second side of [the] said at least one pair of opposite sides, and at least part of the chip connection portions are common to the plurality of predetermined types of semiconductor chips so as to be used for input/output of signals having identical specifications.